Amendments to the Specification:

The title of the invention is objected to because it is allegedly not indicative of the invention to which the claims are directed. Please amend the title to read:

"APPARATUS AND METHOD TO GENERATE A REPAIR SIGNATURE FOR REPAIRING A MEMORY"

The specification is objected to because pages 2 and 3 of the specification have discussed the element **"external test solution 106"** but it can't be found in the drawings. Please replace paragraph [004] with the following amended paragraph:

[004] Figure 1 illustrates a block diagram of a previous technology to generate a repair signature for an embedded memory possessing a redundancy structure used in a system on a chip (SoC). SoC **102** integrates on-chip memory **104** with processors and other similar components, all on the same chip, to decrease cost and increase performance. Redundancy techniques include adding extra memory rows and memory columns that can be substituted for defective components within the memory. The prior external test solution ~~**106**~~ creates a hard repair signature under one set of conditions. The single set of conditions is typically standard operating temperature and voltage.

In addition, please replace paragraph [006] with the following amended paragraph:

[006] The typical external test solution ~~106~~ limits the detection of defective components to defects occurring during the manufacturing process and at standard environmental conditions and not defects that occur after the SoC is in operation or atypical environmental conditions such as high and low temperatures, high and low levels of operating voltages, high and low frequency conditions, etc. Further, the typical external solution may run a first test algorithm to determine defects in the memory or a second test algorithm to determine the defects in the memory. Test algorithms are typically rated to detect a given percentage of the actual defects that exist in a memory, such as 95% effective or 99 % effective. The manufacturer may then choose to apply the results of the first test algorithm or the second test algorithm to repair a memory. However, no way exists to compare the results of the first test algorithm and the second test algorithm to repair all the defects detected by either the first test algorithm and the second test algorithm. Also, memory tester **108** may not be able to test the memories at the speed of the chip. Thus, potential defects that only occur when the memory is operating at speed may not be detected.

The drawings have been objected to because the specification refers to Figure 4d, however Figure 4d is not shown in the drawings. Accordingly, please replace paragraph [008] with the following amended paragraph:

[008] The drawings refer to the invention in which:

figure 1 illustrates a block diagram of a previous technology to generate a repair signature for an embedded memory possessing a redundancy structure used in a system on a chip (SoC);

figure 2a illustrates an embodiment of a block diagram of one or more memories with each memory having one or more redundant components associated with that memory and a processor containing reconfiguration logic to generate an augmented repair signature;

figure 2b illustrates a flow diagram of generating multiple exemplary augmented repair signatures;

figure 3 illustrates an embodiment of a block diagram of a processor containing multiple engines such as a built in self-test engine, a built-in self-diagnosis engine, a built-in redundancy allocation engine, and reconfiguration logic;

figure 4a illustrates an embodiment of a block diagram of the Built-in Redundancy Allocation (BIRA) engine examining information from a database to create a repair signature;

figure 4b illustrates various embodiments of exemplary repair signatures;

figure 4c ~~and figure 4d illustrate~~ illustrates a flow diagram of an embodiment to augment an existing repair signature;

figure 5 illustrates a block diagram of an embodiment of one or more processors to test and repair several memory instances, either running in parallel or one at a time;

figure 6 illustrates a block diagram of an embodiment of a memory;

figure 7 illustrates an embodiment of a block diagram of a memory array split into banks and redundant components associated with that memory array;

figure 8 illustrates an embodiment of a block diagram of the built in redundancy engine having a plurality of registers;

figure 9 illustrates a block diagram of an embodiment of a testing pattern for an embodiment of a BIRA algorithm;

figure 10 illustrates an embodiment of an exemplary starting condition for the BIRA registers in generating an augmented repair signature;

figure 11 and figure 12 illustrate an exemplary use of a first BIST algorithm and a first BIRA algorithm using the first pass to detect errors and perform redundancy allocation in the memory array;

figure 13 and figure 14 illustrate the BIRA algorithm attempting to repair additional defects detected by a second test in order to augment the first repair signature; and

figure 15 and figure 16 illustrate the BIRA algorithm attempting to repair cumulative defects detected by a third test in order to augment the second repair signature.

In addition, please replace paragraph [041] with the following amended paragraph:

[0041] Figure 4c ~~and figure 4d illustrate~~ illustrates a flow diagram of an embodiment to augment an existing repair signature. In an embodiment, the reconfiguration logic or another similar logic block performs these operations.